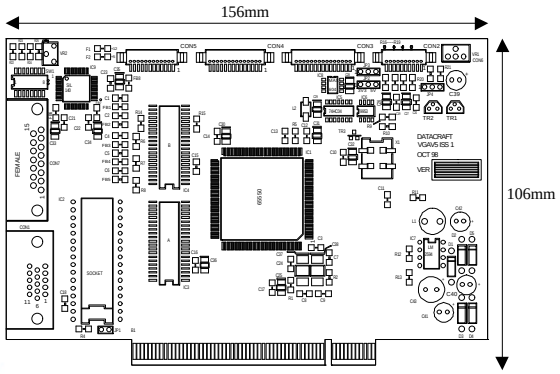
VGAV5



The VGAV5 is a PCI board designed to drive both CRT and LCD displays. It is based on the highly versatile Chips and Technologies 65550 IC and provides a cost effective solution for driving graphics LCD displays.

FEATURES:

- **HiQ32/64 Video LCD controller 65550.**
- **PanelLink™ Sil. 140 interface, up to 10 meter drive distance. Also available from Datacraft are cable solutions and PanelLink termination board RXBV1 (Sil 141).**
- **Support for a wide range of LCD panels including: TFT, STN dual and single scan in both monochrome and colour.**
- **Panel resolutions including: 320x240, 640x480,800x600, 1024x768 and 1280x1024.**
- **Full 24 bit colour interface capability.**
- **2MB display memory as standard.**
- **3.3V and 5V panel interface.**
- **Simultaneous driving of both CRT and LCD.**
- **Hardware switching of up to 32 BIOS set-ups.**
- **Power up and down sequencing for safe panel operation.**
- **Optional +Ve & –Ve voltage generation for LCD BIAS.**
- **Optional Temperature compensation for STN displays.**

INTERFACE CONNECTION

CON1 CRT interface.

15 pin high density female Dtype with screw locks.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	Red	9	NC
2	Green	10	GND
3	Blue	11	NC
4	NC	12	NC
5	GND	13	Hsync
6	Red Gnd	14	Vsync
7	Green Gnd	15	NC
8	Blue Gnd		

CON2,3,4,5 LCD interface.

Molex 53261-xx90. CON2 xx=10, CON3 xx=15, CON4 xx=14, CON5 xx=12.

CON2	SIGNAL	CON3	SIGNAL	CON4	SIGNAL	CON5	SIGNAL
1	+VEE Safe	1	LD3(P4)	1	P8	1	P20
2	GND	2	LD2(P5)	2	P9	2	P21
3	VDD Safe	3	LD1(P6)	3	P10	3	P22
4	+12V Safe	4	LD0(P7)	4	P11	4	P23
5	GND	5	UD3(P0)	5	GND	5	GND
6	Pot-	6	UD2(P1)	6	P12	6	M
7	Pot Wiper	7	UD1(P2)	7	P13	7	ENAVEE
8	Pot+	8	UD0(P3)	8	P14	8	GND
9	Therm-	9	VEE/Vcon	9	P15	9	VDD Safe
10	Therm+	10	GND	10	GND	10	+12V Safe
		11	VDD Safe	11	P16	11	+5V out
		12	ENABLK	12	P17	12	NC
		13	Clock	13	P18		
		14	LP	14	P19		
		15	FLM				

CON6 Contrast Potentiometer connection.

3 pin 0.1” pitch header or on board pot.

PIN NUMBER	SIGNAL
1	Pot left
2	Pot wiper
3	Pot right

INTERFACE CONNECTION

CON7 PanelLink interface.

15 pin female Dtype with screw locks.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	TX2+	9	GND
2	TX2-	10	GND
3	TX1+	11	+12V Safe
4	TX1-	12	GND
5	TX0+	13	+5V out
6	TX0-	14	GND
7	TXC+	15	GND
8	TXC-		

JUMPER LINK DETAILS

JP1: 1&2 BIOS EPROM IC2 A16= low when linked and high when not linked.

JP2: 1&2&3 Panel interface voltage selection: Link 1&2 for 3.3V or link 2&3 for 5V.

JP3: 1&2&3 Con3 pin 9 VEE/Vcon voltage selection: Link 1&2 for VEE via TR1 or TR2 or link 2&3 for pot wiper connection.

JP4: 1&2&3 Pot- connection: Link 1&2 for connection to –VEE via R20 or link 2&3 for connection to GND via R21.

SELECTOR SWITCH DETAILS

SW2

This is a bank of 4 switches placed on the back of the PCB. They are used for the selection of different BIOS set-ups as follows:

SW2	PANEL (40K BIOS)	SW2	PANEL (44K BIOS)
0000	1024X768 Dual scan STN colour	1000	800x600 TFT colour
0001	1280x1024 TFT colour	1001	800x600 TFT colour
0010	640x480 Dual scan STN colour	1010	800x600 Dual scan STN colour
0011	800x600 Dual scan STN colour	1011	800x600 Dual scan STN colour
0100	640x480 Sharp TFT colour	1100	1024x768 TFT colour
0101	640x480 18-bit TFT colour	1101	1024x768 TFT colour
0110	1024x768 TFT colour	1110	Reserved
0111	800x600 TFT colour	1111	Reserved

SW2 Con't

A further bank of 16 BIOS set-ups can be selected via JP1, if a 1Meg BIOS EPROM is utilised. This gives a total of 32 BIOS set-ups which can be selected via hardware switches. These set-ups can be modified to accommodate most customer displays, please contact Datacraft for further information.

SW1 PanelLink configuration switch

This is a bank of 8 switches used to configure the PanelLink interface.

SW1	ACTION
1	Routes P16 of 65550 (IC1) to D16 of Sil140 (IC9).
2	Routes SHFCLK 65550 (IC1) to D16 of Sil140 (IC9).
3	Routes PCLK 65550 (IC1) to D16 of Sil140 (IC9).
4	Routes PCLK 65550 (IC1) to IDCK of Sil140 (IC9).
5	Routes SHFCLK 65550 (IC1) to IDCK of Sil140 (IC9).
6	PD. ON = Powered down mode. OFF = Normal operation.
7	CEDGE. ON = Control signals latched on falling edge of IDCK. OFF = Control signals latched on rising edge of IDCK.
8	DEDGE. ON = Data is latched on falling edge of IDCK. OFF = Data is latched on rising edge of IDCK.

For further information on the PanelLink interface please refer to the SIL140 data sheet.

NOTE: If the PanelLink interface is being used, the panel interface voltage must be set to 3.3V (See JP2). If the Panel interface voltage is set to 5V (JP2), the SIL140 chip must be in power down mode (SW1.6 ON).

VR2 Ext-Swing Control Potentiometer

This is a 2K pot. which controls the voltage swing of the differential outputs of the PanelLink interface.

ELECTRICAL SPECIFICATIONS

SYMBOL	PARAMITER	MIN	TYP	MAX	UNIT
VCC in	LogicSupply voltage	4.5	5.0	5.5	V
+12V in	VEE gen and back light inverter supply voltage	11.0	12.0	13.0	V
VDD Safe out	Switched +5V out to panel	VCC	VCC	VCC	V
IDD Safe out				1.0	A
VEE Safe out	LCD Bias voltage generator	-25		+35	V
IEE Safe out				100	mA
+12V Safe out	Switched +12V out to back light inverter.	+12V in	+12V in	+12V in	V
+12I Safe out				1.0	A
Top	Operating temperature	0		+70	^{o}C
Tstg	Storage temperature	-40		+125	^{o}C