

# VBWV1

DATE	DESCRIPTION OF CHANGE
18/12/02	Replaced page2 picture of board ident with issue 2 version.
"	Added Transfer compressed block command (1C).
"	Added addressability to board operation.
"	Added DC4 reply to commands 17,18,1B.
"	Added software ident register to internal E <sup>2</sup> memory.
"	Added baud rate selection to internal E <sup>2</sup> memory.
"	Added I <sup>2</sup> C rate selection to internal E <sup>2</sup> memory.
"	Added board address to internal E <sup>2</sup> memory.
"	Updated backlight voltage values.

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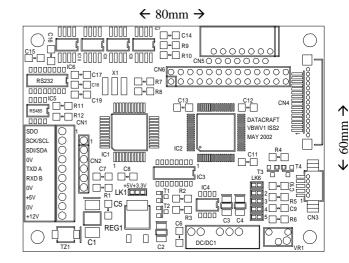


# $D \land T \land CR \land FT$

**VBWV1** is part of the **VIEW BY WIRE™** range of display driver boards aimed at enabling small to medium monochrome and colour displays to be driven from low cost serial interfaces.

## **VBWV1 Features ¬**

- Epson display controller with 80K byte of embedded SRAM.
- Drives active matrix TFT and Passive single and dual scan displays. Up to 640 x 480 resolution.
- 1/2/4/8 bit-per-pixel (bpp) colour depth support.
  640x480 at 2bpp
  640x240 at 4bpp
  320x240 at 8bpp



Depth 14mm Max

- Up to 16 shades of grey on monochrome panels.
- Hardware portrait mode enabling direct hardware 90° rotation of display image.
- 3.3V and 5V panel support.
- RS232 (Optional RS485, I<sup>2</sup>C and SPI) interfaces.
- LCD VEE voltage generation on board with contrast adjustment.
- Up to 128K byte of E<sup>2</sup>prom on board for picture storage. (32K Standard).
- Character set built in to microcontroller flash memory.
- Character size 8x8 and 8x16 available.
- Foreground and background character colour attributes.
- Direct write and character write modes.
- Block transfer of graphics data from E<sup>2</sup> memory to display memory.
- Storage of Display controller set-up registers and look up table in microcontroller internal E<sup>2</sup> memory enabling automatic display initialisation on power up.
- On board Flash based in circuit programmable microcontroller for easy updates and customisation. (Interface directly to MPLAB® ICD via CN2).

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### **Interconnection details**

CN1 Interface and power				
conne	ection			
Mole	X			
22-05	5-1102			
PIN	SIGNAL			
1	SDO			
2	SCK/SCL (I <sup>2</sup> C)			
3	SDI/SDA (I <sup>2</sup> C)			
4	0V			
5	TXD (RS232 / RS485A)			
6	RXD (RS232 / RS485B)			
7	0V			
8	+5V In			
9	0V			
10	+12V/+5V In (For			
	backlight inverter.)			

CN2 Programming interface for firmware updates. 0.1" Header				
PIN	SIGNAL			
1	PGM			
2	PGC			
3	PGD			
4	0V			
5	+5V			
6	VPP			

CN3	CN3 Backlight inverter interface				
Mole	Molex				
53261	1-0590				
PIN	SIGNAL				
1	+12V/+5V Safe (switched				
	via LCDPWR pin.) Origin =				
	CN1 pin 10				
2	0V				
3	+5V Safe (switched via				
	LCDPWR pin.)				
4	Dim use R4 to set backlight				
	brightness.				
5	Dim use R4 to set backlight				
	brightness.				

CN4	Colour STN display
interf	
1mm	pitch FFC
PIN	SIGNAL
1	FPFRAME
2	FPLINE CL1
3	FPSHIFT CL2
4	LCDPWR
5	+5V/3.3V
6	0V
7	VEECON
8	FPD0
9	FPD1
10	FPD2
11	FPD3
12	FPD4
13	FPD5
14	FPD6
15	FPD7
16	0V

CN5	Monochrome display			
interface.				
Mole	X			
52044	4-1445			
PIN	SIGNAL			
1	FPD4			
2	FPD5			
3	FPD6			
4	FPD7			
5	LCDPWR			
6	FPFRAME			
7	NC			
8	FPLINE			
9	FPSHIFT			
10	+5V/3.3V			
11	0V			
12	VEE-			
13	VEECON			
14	0V			

CN6 General Purpose Display Connection							
26 W	26 Way IDC						
PIN	SIGNAL	PIN	SIGNAL				
1	VEE+	2	VEE-				
3	VEECON	4	+12V Safe				
5	+5V/3.3V	6	+5V/3.3V				
7	0V	8	FPSHIFT				
9	0V	10	LCDPWR				
11	DRDY	12	FPFRAME				
13	FPLINE	14	FPD0				
15	FPD1	16	FPD2				
17	FPD3	18	FPD4				
19	FPD5	20	FPD6				
21	FPD7	22	FPD8				
23	FPD9	24	FPD10				
25	FPD11	26	GPIO				

# Link details

LK1	
Solder 1	Link
LINK	SIGNAL
1&2	+5V Display
2&3	3.3VDisplay

LK1 sets the operating voltage to either 5V or 3.3V. Note this also affects the SPI and  $I^2C$  interfaces.

LK2-6				
Solder l	Link <u>One only</u>			
LINK	SIGNAL			
2	For +VEE			
	35V			
3	For +VEE			
	42V			
4	For +VEE			
	30V			
5	For –VEE			
	-30V			
6	For +VEE			
	5V			

LK2-6 sets the LCD VEE voltage level. These affect the VEE+ VEE- and VEECON levels as shown in the table. Note: link only one if the DC/DC converter is fitted.

For displays with a contrast voltage between 0V and 5V remove the DC/DC converter and link 6 and 4. VR1 will then control the VEECON voltage between 0V and 5V. The swing can be further restricted by increasing R6 and R5.



### **Command summary**

Stx=02h Etx=03h Data=00h to ffh Ack=06h Nak=15h Dc4=14h Null=00h

Command	Hex	Sequence	
Graphics mode.	10	Stx,address,10,datadata,etx,etx	
External EE memory mode.	11	Stx,address,11,datadata,etx,etx	
Set writing address to Display.	12	Stx,address,12, address0-7, address8-15, address16, etx,etx	
Set writing address to EE mem.	13	Stx,address,13, address0-7, address8-15, address16-24,	
		etx,etx	
Transfer block from EE mem to	14	Stx,address,14, width0-7, width8-15, height0-7, height8-15,	
display.		etx,etx	
Read internal EE memory.	15	Stx,address,15,address,address,,etx,etx	
Write 1375 set-up data to	16	Stx,address,16, address, datadata, etx,etx	
internal EE memory.			
Initialise 1375 registers.	17	Stx,address,17, etx,etx	
Character mode.	18	Stx,address,18, datadata, etx,etx	
Set writing position.	19	Stx,address,19, x-data, y-data, etx,etx	
Set character attribute.	1A	Stx,address,1A, size-data, foreground-colour-data,	
		background-colour-data, etx,etx	
Clear all display memory	1B	Stx,address,1B, etx,etx	
Transfer compressed block from 1C		Stx,address,1C, width0-7, width8-15, height0-7, height8-15,	
EE mem to display.		etx,etx	

# **Protocol description**

Data is sent to the VBWV1 board in packets framed with Stx (02h) and Etx Etx (03h 03h). The Byte following the Stx character is the board address 00 to FFh, this enables several boards to be on one bus. Sending address 00 will access all boards regardless of their address value. The Byte following the address defines the command. To prevent false end of packet sequences occurring in data being sent the following action should be taken: If Etx (03h) occurs in the data, the transmitter should send a Null (00h) character after it, the receiver then detects this 03h 00h sequence removes the 00h and writes 03h as data. This ensures genuine end of packet sequences and general data are distinguishable.

After the end of packet sequence Etx Etx an Ack(06h) character is transmitted to confirm success. If an error occurred then a Nak(15h) character is transmitted.

#### **Command description**

#### **Graphics Mode 10h**

After the 10h command any amount of data can be sent which will be stored in display memory starting at the address set by command 12h. The address is auto-incremented after each write.

#### External E<sup>2</sup> Memory Mode 11h

After the 11h command any amount of data can be sent which will be stored in external  $E^2$  memory starting at the address set by command 13h. The address is auto-incremented after each write. Also after each write a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

# Set writing address to Display 12h

The three bytes following the 12h command define the display memory writing address. In the order Address0\_7, Address8\_15, Address16. Note only the first bit in byte three is used as the address range is A0 to A16.

#### Set writing address to $E^2$ Memory 13h

The three bytes following the 13h command define the E<sup>2</sup> memory writing address. In the order Address0\_7, Address8\_15, Address16-24. Note Address16-24 is included for future increases in memory size.



Transfer block from E<sup>2</sup> memory to Display memory 14h

The four bytes following the 14h command define the width and height of the block to be transferred as follows: The first two bytes width0\_7 and width8\_15 define the block width in bytes -1, ie. At 4bpp a width value of 23 will give a pixel width of 48. The second two bytes height0\_7 and height8\_15 define the block height in pixels-1. Ie. A height value of 47 will give a height of 48 pixels.

Before executing this command the set writing address commands 12h and 13h should be set. After completion, a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

Read internal E<sup>2</sup> memory 15h

The command 15h enables data to be read from the Microcontroller internal E<sup>2</sup> memory. Address bytes following the command are replied to with the data at that address. Etx,etx ends the command

Initialise controller registers 17h

The command 17h initialises the controller registers and look up table, from the Microcontroller internal E<sup>2</sup> memory, a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

#### Character Mode 18h

After this command 18h data is accepted as ASCII character data and characters are written to the display. Back space 08h, Carriage return 0Dh and Line feed 0Ah are also interpreted. After each character a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure. The character set is stored in the Microcontroller flash memory and can easily be modified. Please contact supplier for more details.

#### Set character writing position 19h

The two bytes following the 19h command define the X and Y positions in characters (8x8) where the next character will be written. (0,0 = top left).

#### Set character attributes 1Ah

The three bytes following the 1Ah command define the character attributes as follows: Character size 0 for 8x8 and 1 for 8x16. Foreground colour byte. Background colour byte. Default is 00h, 0Fh, 00h.

#### Clear all display memory 1Bh

All display memory is filled with 00h, a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

## Transfer compressed block from E<sup>2</sup> memory to Display memory 1Ch

This command operates the same as command 14h except the transfer routine assumes compressed image data (8 bit RLE used). For certain types of image where there are large blocks of the same colour compression improves both speed and memory space used.



Write controller set-up data to internal  $E^2$  memory 16h The command 16h enables data to be written to the Microcontroller internal  $E^2$  memory. This memory holds display register, colour look up table and interface set-up information. This is used to configure the board on power-up or after command 17h. The first byte following the command defines the address, which is then followed by data. The address auto-increments after each write and a DC4 (14h) character is transmitted after each byte to confirm success.

The correspondence between the internal  $E^2$  memory and display controller registers are defined in the

following table:

following table:			
Internal E <sup>2</sup>	Display	Example value	Register description.
memory	controller	for 320 x 240	•
address	register	colour STN at 4	
	value	Bpp (16 colours)	
00h	01h	27h	Mode register 0
01h	02h	80h	Mode register 1
02h	03h	03h	Mode register 2
03h	04h	27h	Horizontal panel size register = (width in pixels/8)-1
04h	05h	Efh	Vertical panel size (lsb) –1
05h	06h	00h	Vertical panel size (msb)
06h	07h	00h	Fpline start position.
07h	08h	00h	Horizontal non-display period.
08h	09h	00h	Fpframe start position.
09h	0Ah	05h	Vertical non-display period.
0Ah	0Bh	00h	Mod rate register.
0Bh	0Ch	00h	Screen1 start address register (lsb).
0Ch	0Dh	00h	Screen1 start address register (msb).
0Dh	0Eh	00h	Screen2 start address register (lsb).
0Eh	0Fh	00h	Screen2 start address register (msb).
0Fh	10h	00h	Screen1 start address register overflow (A16).
10h	11h	00h	Memory address offset register.
11h	12h	FFh	Screen1 vertical size register (lsb).
12h	13h	03h	Screen1 vertical size register (nsb).
13h	18h	00h	
1311 14h		00h	GPIO configuration control register.
	19h		GPIO status / control register.
15h	1Ah	00h	Scratch pad register.
16h	1Bh	00h	Swivel view mode register.
17h	1Ch	00h	Swivel view line byte count register.
18h,19h,1Ah	17h	00h,00h,00h	Look up table RGB index value 00 (black).
1Bh,1Ch,1Dh	17h	80h,00h,00h	Look up table RGB index value 01 (dark red).
1Eh,1Fh,20h	17h	00h,80h,00h	Look up table RGB index value 02 (dark green).
21h,22h,23h	17h	80h,80h,00h	Look up table RGB index value 03 (dark yellow).
24h,25h,26h	17h	00h,00h,80h	Look up table RGB index value 04 (dark blue).
27h,28h,29h	17h	80h,00h,80h	Look up table RGB index value 05 (dark magenta).
2Ah,2Bh,2Ch	17h	00h,80h,80h	Look up table RGB index value 06 (dark cyan).
2Dh,2Eh,2Fh	17h	B0h,B0h,B0h	Look up table RGB index value 07 (light grey).
30h,31h,32h	17h	70h,70h,70h	Look up table RGB index value 08 (dark gray).
33h,34h,35h	17h	F0h,00h,00h	Look up table RGB index value 09 (light red).
36h,37h,38h	17h	00h,F0h,00h	Look up table RGB index value 10 (light green).
39h,3Ah,3Bh	17h	F0h,F0h,00h	
		, ,	Look up table RGB index value 11 (light yellow).
3Ch,3Dh,3Eh	17h	00h,00h,F0h	Look up table RGB index value 12 (light blue).
3Fh,40h,41h	17h	F0h,00h,F0h	Look up table RGB index value 13 (light magenta).
42h,43h,44h	17h	00h,F0h,F0h	Look up table RGB index value 14 (light cyan).
45h,46h,47h	17h	F0h,F0h,F0h	Look up table RGB index value 15 (white).
48h	Na	9Fh	Display block on power up width0-7
49h	Na	00h	Display block on power up width8-15
4Ah	Na	EFh	Display block on power up height0-7
4Bh	Na	00h	Display block on power up height0-15
4Ch	Na	1Fh	Software identification low byte (Checksum used)
4Dh	Na	8Ch	Software identification high byte (Checksum used)
4Eh	Na	04h	Serial Baud rate 0=9600, 1=19200, 2=38400,
	- '''	J	3=57600, 4=115200.
4Fh	Na	01h	I <sup>2</sup> C rate 0=normal (LC chips) 1=fast (FC chips)
50h	Na	00h	Board address. 00 to FFh. (Avoid address 03h)
5011	114	0011	Dourd address. Of to 11 II. (Avoid address UJII)

**Note:** For displays requiring 8Bpp (256 colour) the remainder of the look up table will need to be loaded via the serial interface, directly into the display controller.

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If the address 48h has any value other than FFh then a transfer compressed block command is carried out on power-up using the width and height values in the internal  $E^2$  memory from 48h to 4Bh.

Address 4Ch and 4Dh contain the PIC software checksum for identification purposes.

Address 4Eh contains the serial baud rate set at power-up, 0=9600, 1=19200, 2=38400, 3=57600, 4=115200.

Address 4Fh contains the I<sup>2</sup>C rate set at power-up, 0=normal (LC chips) 1=fast (FC chips).

Address 50h contains the board address. The board will respond to commands when the address sent corresponds to the value storred at this location or the address sent is 00h. Avoid using address 03h as it can conflict with the end of packet character.

# RS232 / RS485 Interface

Format:

Baud rate: 19200 (default)

Data: 8 bits Parity: None Stop bits: 1

The RS485 interface is available as an option in place of the RS232 interface, contact Datacraft for more details.

## I<sup>2</sup>C Interface

The  $I^2C$  bus is connected to the on board  $E^2$  memory IC's 7-10 (Address 00 to 03) and the microcontroller. This enables direct access to the  $E^2$  memory if required and fast access to the microcontroller. For further details contact Datacraft.

#### **Electrical specification**

SYMBOL	PARAMITER	MIN	TYP	MAX	UNIT
VCC in	LogicSupply voltage	4.5	5.0	5.5	V
+12V in	Back light inverter supply voltage	0.0	12.0	15.0	V
VDD Safe out	Switched +5V out	VCC	VCC	VCC	V
IDD Safe out				1.0	A
VEE +/-	LCD Bias voltage	-30		+42	V
IEE +/-				30	mA
VEECON	LCD Contrast voltage adjusted via VR1 LK2 made.	1		34	V
VEECON	LK3 made. +12V in must be present.	1		41	V
VEECON	LK4 made.	1		29	V
VEECON	LK5 made.	-29		-1	V
+12V Safe out	Switched +12V out to back light inverter.	0.0 in	+12V in	+15V in	V
+12I Safe out				1.0	A
Top	Operating temperature	0		+70	°C
Tstg	Storage temperature	-40		+125	°C

#### **Further information**

Please refer to the Epson S1D13705 Specification for further details of the features available.

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# **Character set**

HEX	0.0	10	20	30	40	50	60	70	80	90	A0	В0	C0	D0	ΕO	F0
0.0				0	a	P	^	F	Ë	2			À	Ð	à	ð
01			!	1	A	Q	.⊟	-=	4	Ω	i	+	Á	N	á	ñ
02			11	2	В	R	b	<b>F</b>	f	*****	¢	2	Ā	Ò	ā	ò
03			#	3	C	5	i	=	1.	×	£	Э	Ā	Ó	-	ó
04			\$	4	D	T		†;	Ŀ		Ø	*	Ä	ō	-==	ō
05			7,	5	E				08	0	#	P	Å	ō		ō
06			8.	6	-	Ų	£	Ų		Ç	i	1	Æ	ö		Ö
07			2	7	G	IJ	-	IJ	ð		\$	-	Ç	×	Ç	
08			(	8	-	X	H	×	4	$\leq$	••	.,	È	ø	è	φ
09			)	9	I	Y		Y	h.	<u>\</u>		1	É	Ù	é	Ù
0 A			*	::	J	Z	j	Z	Θ	非	₫		Ē	Ú	Ē	Ó
0В		,	-	;	K	L	k	<	À,	Ţ	\$	<b>%</b>	Ë	Ū	ë	Ü
0C				$\leq$		٧,	1	i	Л	8	*****	ķ	Ì	ij	ì	ü
0D					M	]	M	3	T	Ĵ		12	Í	φ	í	ý
ΟE				>	H	^	m		ф	(0)	0		Ī	þ	ī	þ
0F			/	9			O	¥	(0)	$\ddot{\otimes}$	*****	Ċ	Ï	β	ï	ÿ

As the character set is stored in the microcontroller flash memory it is easily modified for custom characters. Please contact Datacraft for further details.