Step by Step VBWV1 Set-up instructions (Issue 3 board):

Before connecting power to the VBWV1 board the various links need to be configured depending on the particular display being driven.

1) Set LK1 the 5V / 3.3V link according to the display voltage required.

2) Links 2 to 7 will need to be configured according to the voltage required.

LK2-7 2mm Jumper Link Two only	
LINK	SIGNAL
2 & 7	For +VEE 29V
3 & 7	For +VEE 36V
4 & 7	For +VEE 24V
5 & 7	For -VEE –24V
6 & 7	For -VEE -19V
6 & 4	For +VEE 5V

These voltages assume a +12V / -12V DC/DC converter is used and in the case of Link 3 the 12V supply is also connected. A +15V / -15V DC/DC converter can also be used to obtain higher voltages.

3) Without a display attached supply 5V to the board and connect to a PC serial port as indicated in the Visual Basic Windows Application software document.

4) Using the Windows application software "Modify registers" screen configure the board for the particular display with the required number of colours etc. as follows:

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Display controller register settings

Working out the register settings for a particular display is not as difficult as it may first appear. Most of the settings can be 00 for basic operation and example values are given for the essential settings.

Register 01 Mode 0

This register must be set for correct display operation.

Example values :
320 x 240 Mono STN 4 bit: 04h
640 x 480 Mono STN Dual 8 bit: 45h
320 x 240 Colour STN single 8 bit format 2: 27h

Register Address 1FFE1h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reg 01 Mode0	TFT / STN	Dual / Single scan	Colour / Mono	Fpline polarity	Fpframe polarity	Fpshift mask	Data width bit 1	Data width bit 0

Bit 7 0 = STN. 1 = TFT.
Bit 6 0 = single scan display. 1 = Dual scan display.
Bit 5 0 = Mono display. 1 = Colour display.
Bit 4 0 = Active low Fpline. 1 = Active high Fpline.
Bit 3 0 = Active low Fpframe. 1 = Active high Fpframe.
Bit 2 0 = Fpshift not masked. 1 = Fpshift masked during none display periods.
Bit 1 Display interface data width Bit 1 see table below:
Bit 0 Display interface data width Bit 0 see table below.

TFT / STN Reg 01 Bit 7	Colour/Mono Reg 01 Bit 5	Dual / Single Reg 01 Bit 6	Data width Bit 1 Reg 01 Bit 1	Data width Bit 0 Reg 01 Bit 0	Function
0	0	0	0	0	Mono single 4bit passive LCD.
				1	Mono single 8bit passive LCD.
			1	0	Reserved
				1	Reserved
		1	0	0	Reserved
				1	Mono dual 8bit passive LCD.
			1	0	Reserved
				1	Reserved
	1	0	0	0	Colour single 4bit passive LCD.
				1	Colour single 8bit passive LCD format 1.
			1	0	Reserved
				1	Colour single 8bit passive LCD format 2.
		1	0	0	Reserved
				1	Colour dual 8bit passive.
			1	0	Reserved
				1	Reserved
1	Don’t care.			0	9-bit TFT panel.
				1	12-bit TFT panel.

Register 02 Mode 1

This register must be set for correct display operation.

Example values :
320 x 240 Mono STN Black and white: 30h
640 x 240 Mono STN 16 grey scales: 80h
320 x 240 Colour STN 16 colour: 80h

Register Address 1FFE2h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reg 02 Mode1	Bit-per-pixel Bit 1	Bit-per-pixel Bit 0	High performa-nce	Input clock divide.	Display blank	Frame repeat	Hardware Video invert enable	Software Video invert

Bit 7 Colour / Grey scale depth Bit 1. See table below:
Bit 6 Colour / Grey scale depth Bit 0. See table below:
Bit 5 0 = Normal performance. 1 = High performance (MClk = PClk).
Bit 4 0 = PClk = CLk(20Mhz) 1 = PClk = CLk/2 (10Mhz).
Bit 3 0 = Normal. 1 = Display blanked.
Bit 2 0 = Normal. 1 = Frame repeat for EL panels.
Bit 1 0 = Normal. 1 = Hardware Video invert enabled on pin FPD11.
Bit 0 0 = Normal Video mode. 1 = Inverse Video mode.

Colour / Mono Reg 01 bit 6	Bits-per-pixel Bit 1 Reg 02 bit 7	Bits-per-pixel Bit 0 Reg 02 bit 6	Display Mode	
0	0	0	2 Grey scale	1 bit-per-pixel
		1	4 Grey scale	2 bit-per-pixel
	1	0	16 Grey scale	4 bit-per-pixel
		1	Reserved	
1	0	0	2 colour	1 bit-per-pixel
		1	4 colour	2 bit-per-pixel
	1	0	16 colour	4 bit-per-pixel
		1	256 colour	8 bit-per-pixel

Register 03 Mode 2

This register must be set for correct display operation.

Example value:
Usually set to 03h for most displays.

Register Address 1FFE3h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reg 03 Mode2	N/a	N/a	N/a	N/a	LCDPWR Override	Hardware power save enable.	Software power save bit 1.	Software power save bit 0.

Bit 3 0 = Normal. 1 = LCDPWR pin forced low disabling display.
Bit 2 0 = Normal. 1 = Enable Hardware power save pin GPI0.
Bit 1 & Bit 0 00 = Software power save mode. 11 = Normal operation.

Register 04 Horizontal Panel size register

This register must be set for correct display operation.

Example values:
320 x 240 (320 / 8)-1 = 39 (27h)
480 x 320 (480 / 8)-1 = 59 (3bh)
640 x 240 (640 / 8)-1 = 79 (4fh)

Register Address 1FFE4h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Horizontal panel size register.	N/a	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bits 6:0 Determines the horizontal resolution of the display.
Horizontal panel size register = (Horizontal pixel resolution / 8) - 1

Register 05 & 06 Vertical Panel size register

These registers must be set for correct display operation.

Example values:
320 x 240 240 - 1 = 239 (efh)
480 x 320 320 - 1 = 319 (13fh)

Register Address 1FFE5h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Vertical panel size register (LSB).	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Register Address 1FFE6h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Vertical panel size register (MSB).	N/a	N/a	N/a	N/a	N/a	N/a	Bit 9	Bit 8

Bits 9:0 Determines the Vertical resolution of the display.
Vertical panel size register = Vertical pixel resolution – 1

Register 07 Fpline start position

This register is only used for TFT displays.

Example value:
Usually set to 00h for STN displays.

Register Address 1FFE7h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Fpline start position register.	N/a	N/a	N/a	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bits 4:0 Determines the position of the Fpline pulse.
Fpline position (pixels) = (Reg 07 / 2) x 8.

Register 08 Horizontal non-display period

This register is useful for adjusting the frame rate.

Example value:
Any value between 00 and 1fh

Register Address 1FFE8h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Horizontal non-display period	N/a	N/a	N/a	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bits 4:0 Determines the Horizontal non-display period i.e adds time between lines.
Horizontal non-display period (pixels) = (Reg 08 + 4) x 8.

Register 09 Frame start position

This register is only used for TFT displays.

Example value:
Usually set to 00h for STN displays.

Register Address 1FFE9h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Frame start position register.	N/a	N/a	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bits 5:0 Determines the position of the Frame pulse.
Frame position (lines) = Reg 09.

Register 10 (0Ah) Vertical non-display period

This register is useful for adjusting the frame rate.

Example value:
Any value between 03 and 3fh
Experiment with this value to remove horizontal lines on the display.

Register Address 1FFEAh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Vertical non-display period	Status	N/a	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 This bit = 1 during Vertical non-display periods.
Bits 5:0 Determines the Vertical non-display period i.e adds time between Frames.
Vertical non-display period (lines) = Reg 0Ah.

Register 11 (0Bh) Mod rate register

This register is only used for displays with an M input.

Example value:
Any value between 00 and 3fh
Experiment with this value to obtain the best display.

Register Address 1FFEBh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mod rate register.	N/a	N/a	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bits 5:0 Determines the rate at which the M (DRDY/M pin) toggles.
When 00 the M signal toggles every Frame (default). When 01 to 3fh the M signal toggles every Fpline x Reg 0bh.

Register 12 (0Ch) & 13 (0Dh) & 16 (10h) Screen 1 start address

These registers are normally set to 00000 for basic operation.

Register Address 1FFECh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Screen 1 start address register (LSB).	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Register Address 1FFEDh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Screen 1 start address register (MSB).	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Register Address 1FFF0h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Screen 1 start address overflow register.	N/a	N/a	N/a	N/a	N/a	N/a	N/a	Bit 16

Bits 16:0 Determines the starting address of screen1.

Register 14 (0Eh) & 15 (0Fh) Screen 2 start address

These registers are normally set to 00000 for basic operation.

Register Address 1FFEEh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Screen 2 start address register (LSB).	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Register Address 1FFEFh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Screen 2 start address register (MSB).	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Bits 15:0 Determines the starting address of screen2.

Register 17 (11h) Memory address offset register

This register is normally set to 00 for basic operation.

Register Address 1FFF1h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Memory address offset register.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bits 7:0 Determines the offset between the last address of one line and the first address of the following line. Used to create a virtual image.

Register 18 (12h) & 19 (13h) Screen 1 Vertical size register

These registers are normally set to 3FFh for basic operation.

Register Address 1FFF2h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Screen 1 vertical size register (LSB).	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Register Address 1FFF3h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Screen 1 vertical size register (MSB).	N/a	N/a	N/a	N/a	N/a	N/a	Bit 9	Bit 8

Bits 9:0 Determines the vertical size of screen 1. Used for split screen feature.

Registers 21 (15h) & 23 (17h) Look up table registers

These registers affect the colours / grey scales used.

These values can be adjusted using the colour look up table facility in the VBWV1 application software. For monochrome displays only the green values are used.
For 1 Bpp colours 00 – 01 are used.
For 2 Bpp colours 00 – 03 are used.
For 4 Bpp colours 00 – 15 are used.
For 8 Bpp the look up table will need to be written directly from the host system.

Registers 24 (18h) to 28 (1Ch) Various advanced registers

These registers are normally set to 00h for basic operation.

For further information on these register features please refer to the S1D13705 Specification.

Frame rate calculations

To calculate the frame rate use the following formula:
For single scan panels.

$$\text{Frame rate} = \frac{fpclk}{(HDP + HDNP) \times (VDP + VNDP)}$$

For Dual scan panels.

$$\text{Frame rate} = \frac{fpclk}{2 \times (HDP + HDNP) \times (VDP / 2 + VNDP)}$$

Where:
Fpclk = pixel clock (For VBWV1 = 20 Mhz or 10 Mhz if Reg 02 bit 4 (clk1/2) set.
HDP = Horizontal Display Period = (Reg 04 +1) x 8 pixels. I.e for 320 x 240 HDP = 320.
HNDP = Horizontal Non-Display Period = (Reg 08 + 4) x 8 pixels.
VDP = Vertical Display Period = Reg 06 & 05 +1 lines. I.e for 324 x 240 VDP = 240.
VNDP = Vertical Non-Display Period = Reg 0Ah lines.

5) Powering off and on should configure the display controller and enable the VEE contrast voltage. This should be measured with a meter and set to the approximate value using VR1.

6) Power off and connect the display to the board using either CN4, CN5 or CN6. To determined the interconnection you will need the VBWV1 Specification and the Display specification. See the table below to ascertain the data connection relevant for your particular display. Note that CN4 is pin compatible with Hitachi's SX14Q001 ¼ VGA colour STN and CN5 is pin compatible with Hitachi's SP14Q002 ¼ VGA mono display.

SED1375 Pin Name	Monochrome Passive Panel			Color Passive Panel				Color TFT/MD-TFD	
	4-bit Single	8-bit Single	8-bit Dual	4-bit Single	8-bit Single Format 1	8-bit Single Format 2	8-bit Dual	9-bit	12-bit
FPFRAME	FPFRAME								
FPLINE	FPLINE								
FPSHIFT	FPSHIFT								
DRDY	MOD	MOD	MOD	MOD	FPSHIFT2	MOD	MOD	DRDY	
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	LD0	R2	R3
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	LD1	R1	R2
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	LD2	R0	R1
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	LD3	G2	G3
FPDAT4	D0	D4	UD0	D0	D4	D4	UD0	G1	G2
FPDAT5	D1	D5	UD1	D1	D5	D5	UD1	G0	G1
FPDAT6	D2	D6	UD2	D2	D6	D6	UD2	B2	B3
FPDAT7	D3	D7	UD3	D3	D7	D7	UD3	B1	B2
FPDAT8	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	B0	B1
FPDAT9	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	R0
FPDAT10	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	G0
FPDAT11	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4	B0

7) Connect the back light inverter to CN3 according to the VBWV1 Specification. Note that the 12V input on CN1 is fed through a FET switch (controlled by LCDPWR) to CN4 and is used only for driving the inverter. If a 5V inverter is being used simply connect 5V to the 12V input at CN1.

8) Power on and download a picture or dump the character set to the display to check for correct operation. Adjust VR1 for optimum contrast.

9) If the VBWV1 fails to work due to some corruption in the set-up E^2 memory a revert to default settings can be carried out.
With power off the VBWV1 board, link pins 1 & 2 of CN1. Powering the board on with this link set will reset the internal E^2 memory. Remove the link once this has been done.