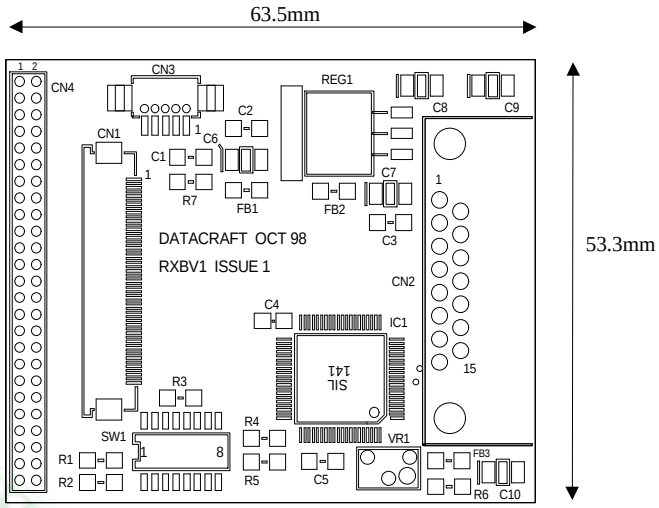
RXBV1

The RXBV1 board forms the receiving end of a PanelLink™ interface. It is based on the Silicon Image Sil 141 IC and provides the ability for display panels from VGA to SVGA to be driven at up to 10 meters from the controller board.



FEATURES:

- **PanelLink™ Sil. 141 RX interface.**
- **Uses TMDS (Transition Minimised Differential Signalling) and on chip termination resistors to reduce EMI.**
- **Support for a wide range of LCD panels including: TFT, STN dual and single scan in both monochrome and colour.**
- **Panel resolutions including: 320x240, 640x480,800x600, 1024x768 and 1280x1024.**
- **Full 24 bit colour 1 bit/pixel mode and 18 bit colour 2 bit/pixel mode (36 bit interface) capability.**
- **Skew and Jitter tolerant for reliable operation.**
- **On board 3.3V regulator and selectable 3.3V / 5V panel voltage.**
- **12V output for back light inverter supply.**
- **Up to 10 meter cable distance when used in conjunction with Datacraft's VGAV5 controller.**

INTERFACE CONNECTION

CN1 and CN4 Panel interface.

The panel interface is brought out on two connectors for flexibility.
CN1 = JAE 50 way 0.5mm pitch FFC.
CN4 = 50 way 2mm pitch DIL header.

PIN NUMBER CN1 and CN4	SIGNAL	PIN NUMBER CN1 and CN4	SIGNAL
1	Panel Vcc	2	Panel Vcc
3	Panel Vcc	4	DE
5	ENABKL	6	LP
7	FLM	8	CLOCK
9	GND	10	Q0
11	Q1	12	Q2
13	Q3	14	Q4
15	Q5	16	GND
17	Q6	18	Q7
19	Q8	20	Q9
21	Q10	22	Q11
23	GND	24	Q12
25	Q13	26	Q14
27	Q15	28	Q16
29	Q17	30	GND
31	Q18	32	Q19
33	Q20	34	Q21
35	Q22	36	Q23
37	GND	38	Q24
39	Q25	40	Q26
41	Q27	42	Q28
43	Q29	44	GND
45	Q30	46	Q31
47	Q32	48	Q33
49	Q34	50	Q35

CN2 PanelLink interface.

15 pin female Dtype with screw locks.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	RX2+	9	GND
2	RX2-	10	BL GND
3	RX1+	11	BL +12V
4	RX1-	12	GND
5	RX0+	13	+5V IN
6	RX0-	14	GND
7	RXC+	15	GND
8	RXC-		

INTERFACE CONNECTION

CON2 Back light inverter interface.

CON2 = 1.25mm pitch Molex 53261-0590.

CON2	SIGNAL
1	BL +12V
2	BL GND
3	+5V out
4	BL BRI
5	BL BRI

Note: Pins 4 and 5 are connected on board via a 47K resistor.

SELECTOR SWITCH DETAILS

SW1 PanelLink configuration switch

This is a bank of 8 switches used to configure the PanelLink interface.

SW1	ACTION
1	Not used.
2	Selects 3.3V panel supply when on.
3	Selects 5V panel supply when on.
4	PD. Power down mode control. ON = Powered down mode. OFF = Normal operation.
5	PIXS. Pixel select. ON = 1 pixel / clock output mode. OFF = 2 pixel / clock output mode.
6	DFO. Data format output control. ON = Continuously running pixel clock for TFT. OFF = Pixel clock gated with DE for DTSN.
7	OCK_INV. ODCK Invert control. ON = Normal ODCK clock. OFF = Inverted ODCK clock.
8	ST. Output drive strength control. ON = Low current drive. OFF = High current drive.

For further information on the PanelLink interface please refer to the SIL141 data sheet.

VR1 Impedance matching control potentiometer.

This is a 2K pot. which enables the impedance matching of the PanelLink cable.This should be adjusted for optimum performance of the panel.

ELECTRICAL SPECIFICATIONS

SYMBOL	PARAMITER	MIN	TYP	MAX	UNIT
+5V in	Logic Supply voltage.	4.5	5.0	5.5	V
BL +12V	Back light inverter supply voltage.	11.0	12.0	13.0	V
Panel Vcc	+5V Panel supply voltage.	4.5	5.0	5.5	V
Panel Vcc	+3.3V Panel supply voltage.	3.13	3.3	3.47	V
Panel Icc	Panel supply current			1.0	A
BL +12I	Back light inverter supply current.			1.0	A
Top	Operating temperature	-25		+105	^{o}C
Tstg	Storage temperature	-40		+125	^{o}C