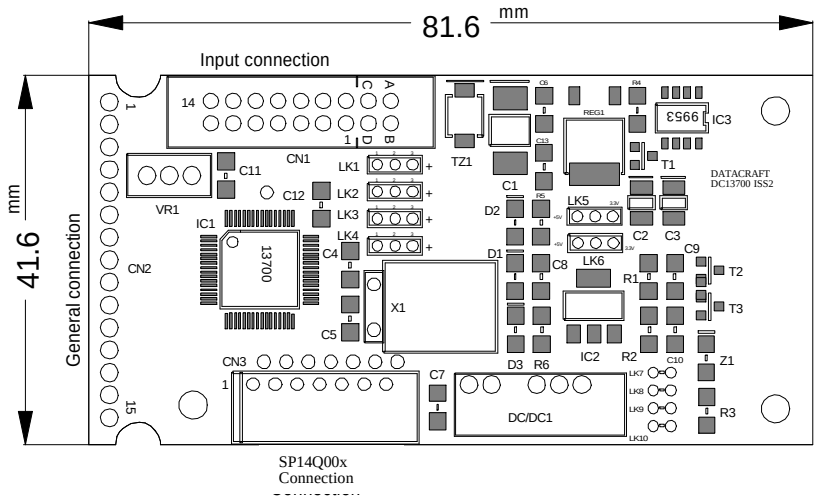
DC13700

DATE	DESCRIPTION OF CHANGE
20/1/06	Now ROHS compliant.
9/1/08	PCB now issue2
--“--	Show Reset pin as active low.
--“--	Updated SP14Qxxx to SP14Q00x
--“--	Updated 6800 bus selection.

The **DC13700** has been designed to drive monochrome graphics LCD modules via a simple 8 bit indirect parallel interface.



DC13700 Features

- Epson S1D13700 display controller with 32K byte of embedded SRAM.
- Drives monochrome single and dual scan displays. Up to 640 x 240 resolution.
- 1/2/4 bit-per-pixel (bpp) Grey scale generation.
  640x240 at 1bpp
  320x240 at 2bpp
  240x160 at 4bpp
- Text, graphics and combined text / graphics display modes.
- Selectable 8 bit 6800 and 8080 host interface.
- 3.3V and 5V host interface and panel support.
- LCD VEE voltage generation on board with contrast adjustment.
- 160, 5x7 pixel characters in character generator ROM (CGROM).
- 64, 8x8 pixel characters in character generator RAM (CGRAM).
- 256, 8x16 pixel characters in character generator RAM.
  (When CGROM not used.)
- Direct connection for Hitachi's SP14Q00x series of displays.
- General purpose connection for 4 bit monochrome LCDs.

Interconnection details

CN1 Host interface and power connection. 2 x 7 0.1" pitch			
PIN	SIGNAL	PIN	SIGNAL
B	0V	A	#Reset cct.
D	S1D13700 #CS	C	S1D13700 #Reset.
1	0V	2	+5V
3	NC	4	A0 / RS
5	R/#W (#WR)	6	E (#RD)
7	D0	8	D1
9	D2	10	D3
11	D4	12	D5
13	D6	14	D7

CN2 General purpose LCD Interface. 15 x 1 0.1" pitch.	
PIN	SIGNAL
1	+5V / +3.3V
2	0V
3	VCON
4	FPLINE (LP)
5	M (WF)
6	YDIS (DISP ON/OFF)
7	YSCL
8	FPFRAME (YD)
9	FPSHIFT (XSCL)
10	RES (XECL)
11	D0
12	D1
13	D2
14	D3
15	VEE (-22V)

CN3 Monochrome display interface. (SP14Q00x compatible) Molex 52044-1445	
PIN	SIGNAL
1	D0
2	D1
3	D2
4	D3
5	YDIS (DISP ON/OFF)
6	FPFRAME (YD)
7	NC
8	FPLINE (LP)
9	FPSHIFT (XSCL)
10	+5V/3.3V
11	0V
12	VEE-
13	VEECON
14	0V

Link 8 & 10 for correct VEE supply.

Jumper Link details

LK1 & LK2 Host interface set-up. 2mm jumper Link.			
LINK	SIGNAL	6800 Host	8080 Host
1	AS	2&3	2&3
2	CNF3	2&3	1&2

LK3 & LK4 Shift clock divide. 2mm jumper Link.		
LK3 CNF1	LK4 CNF0	Clock divide.
Low	Low	4:1 (divide by 4)
Low	High	8:1 (divide by 8)
High	Low	16:1 (divide by 16)

LK5 & LK6 Host and LCD Voltage level. 2mm jumper Link.			
Link	Function	+5V	+3.3V
LK5	LCD interface		
LK6	Host interface		

LK7 to LK10 VEE Set-up 2mm Jumper Link. Link two only	
LINK	SIGNAL
7 & 10	For +VEE +24V
8 & 10	For -VEE -24V
9 & 10	For -VEE -19V
7 & 9	For +VEE +5V

Use the links 7 to 10 to set the required LCD voltage range then use VR1 to adjust the contrast voltage VCON.

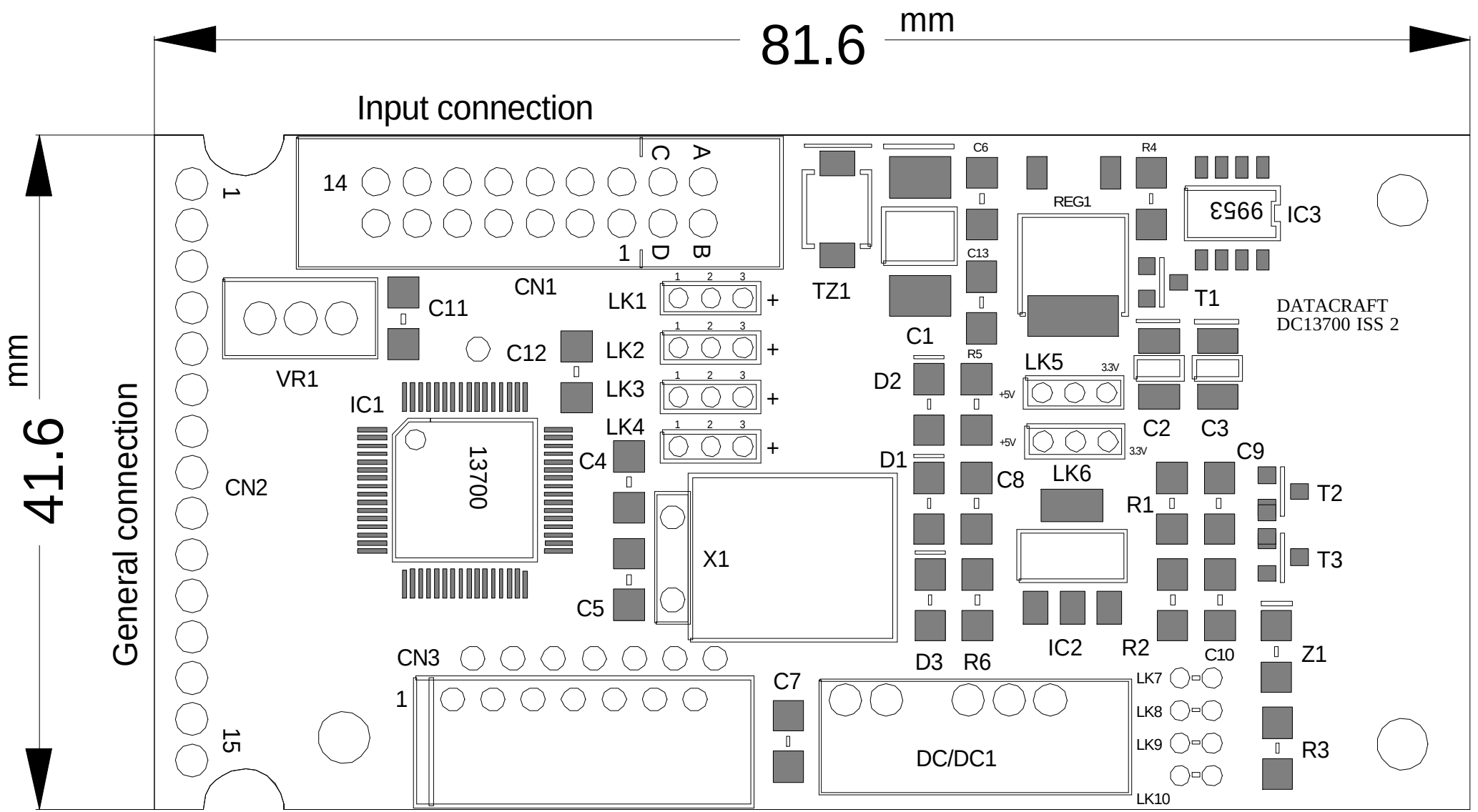
Electrical specification

SYMBOL	PARAMITER	MIN	TYP	MAX	UNIT
VCC in	LogicSupply voltage	4.75	5.0	5.5	V
VEE +/-	LCD Bias voltage	-24		+24	V
IEE +/-				40	mA
VEECON	LCD Contrast voltage adjusted via VR1. LK7 & 10 made.	1		23	V
VEECON	LK8 & 10 made.	-23		-1	V
VEECON	LK9 & 10 made.	-19		4	V
VEECON	LK7 & 9 made.	0.5		4.5	V
Top	Operating temperature	-10		+70	^{o}C
Tstg	Storage temperature	-40		+125	^{o}C

Further information

Please refer to the Epson S1D13700 Specification for further details of the features available.

Visit www.erd.epson.com



SP14Q00x
Connection